REMARKS

Claims 1-22 and 24-40 are pending in the application.

In the Office Action the specification and claims are objected to with regard to the addition of "virtual output queue" (VOQ) as including new matter. It is respectfully submitted the VOQ is fully supported by the original specification and drawings.

For example, the specification describes in page 1 lines 24-25, "logically dividing an input buffer unit per output route". Therefore the input buffer contains virtual queues per output route for example as shown in Figure 3 of applicant's specification. The "logically dividing an input buffer unit per output route (page 1, lines 24-25)" indicates a VOQ (a switch having a plurality of logical queues). The basic structure of the present invention is premised on that a VOQ is used.

In the second embodiment, Fig.43 shows a whole architecture of the present invention. The switch in Fig.43 has the same basic structure of a VOQ switch shown in Fig. 9 of Chao. Fig. 9 of Chao shows a plurality of queues in input line. Chao describes a basic VOQ switch.

Also, Figs. 25, 48, 57, 59, 61, and 66 of the present invention show input buffers having the plurality of queues.

Accordingly, it is respectfully submitted that VOQ is fully supported in the specification.

<u>Prior Art Rejections</u>

Claim 17 is rejected under 35 U.S.C. § 102 (e) as being anticipated by Chao et al. (U.S. 6,449,283) (Chao).

Chao describes a switch with a virtual output queue. Multiple priority levels are discussed in columns 31 and 32. The reference describes that priority levels may be considered

during an input arbitration or during an output arbitration and during an input arbitration the virtual output queue is equal to the number of priority levels multiplied by the number of output ports.

In contrast to Chao, applicant's claim 17 recites: "a scheduler for managing the number of scheduling requests and performing the scheduling from a higher priority class among two or more classes".

In contrast to applicant's claimed invention, the scheduling system of Chao realizes the scheduling at two steps using two kinds of pointers (Arbiter) [Chao-FIG.11].

First, as a request phase, in each input buffer, one VOQ is selected using round robin control by input Arbiter from VOQ in a self-line, and a request is notified to Output Arbiter corresponding to the VOQ.

That is, a request is notified from one input line to only one Output Arbiter.

Next, as a Grant phase, in each Output Arbiter, one input line is selected by round robin from the received requests (= input lines), and the result is notified to the input buffer.

In the system of Chao, in a request phase, in order to notify only one request to a scheduler (Output Arbiter), from one input line, the competition does not occur among the plurality of Output Arbiters that select the same input line.

For this reason, each Output Arbiter can process simultaneously in Chao.

However, Chao fails to disclose "the scheduler for managing the number of scheduling requests and performing the scheduling from a higher priority class among two or more classes".

Claims 1-16, 18-22 and 24-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chao in view of Oba et al. (U.S. 6,262,986).

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Oba describes a packet scheduler with a plurality of packet queues for storing packets. A management unit schedules information specifying the order to read out the packets from the packet queues at the time of packet transmission. Oba describes several scheduling techniques such as the length of the queue, the weight of a corresponding queue, and class scheduling queuing.

The present claimed invention is different from Oba because in the scheduling system of Oba and the scheduling system of the present invention, the purpose, operations and required functions of scheduling are completely different.

First the scheduler of Oba does not need arbitration between lines like an input buffer switch because FIG.10 of Oba shows the scheduler is on an output line.

Oba does not have the competition arbitration function between input lines.

Accordingly, it is respectfully submitted that the scheduling in the input buffer switch that is an object of the present claimed invention is unrealizable by the scheduler of Oba.

Also, the schedule processing unit of Oba aims at impartially selecting queue according to weight given in advance to a plurality of queues supposing the case which has the plurality of queues in certain one line.

Moreover, the method of determining sending out queue as a concrete scheduling method, based on the weight given to each queue with the queue length of each queue is adopted [Oba, column 5, lines 43-48, lines 57-64, column6, lines 30-37].

In contrast, in the present invention, it is premised that there is a plurality of lines each having the plurality of queues (namely, input buffer switch having VOQ). Further, the schedule processing unit of the present invention aims at executing arbitration so that a scheduling result may not compete between lines.

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Moreover, the scheduling processing in the present invention adopts the technique of executing scheduling one by one from a certain input line.

That is, in order to realize fair scheduling, the method of selecting an output line from undecided output lines is adopted by the round robin processing using Intra-highway pointer in the selected input line after selecting a scheduling start input line using Inter-highway pointer (page 10, line 3-6, selecting the output line by unselected by other input line in claim 1).

Thus, as for the schedule processing of Oba, and the schedule processing of the present invention, the purpose and method of the scheduler completely differs each other.

Oba discloses and relates to a scheduling method and apparatus for reading out a packet from a plurality of queues in sequence or in a single line. The structure and control method described in Oba cannot execute scheduling of the input having the VOQ.

In contrast to Oba the present invention provides multiple pointers, for example claim 1 has an inter-highway pointer control unit for indicating the input line where input line scheduling should start and an intra-highway pointer control unit which is a pointer for each input line and indicates for each input line the starting output line where scheduling should begin.

In the scheduling method of Oba, the reading out of the queue is determined by an algorithm based on the present length of the queue and the weight of a corresponding queue (value preset in each queue) at the time of packet arrival and at the time of reading out the packet.

Further, the packet is transmitted from a queue indicating a scheduling result by reading out the scheduling result from a FiFo in each packet time. The scheduling result (object queue number to be read out) is stored in the FiFo of a scheduling unit.

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Oba discloses executing the scheduling process at the time of both packet arrival and reading out the packet and determining a transmission queue using an algorism based on the present length of a queue and the weight of a corresponding queue.

In contrast, in the present invention, the scheduling process is executed only when the packet arrived.

The present invention is characterized by <u>determining an input line for a scheduling object using pointer #1 (inter highway pointer), and determining VOQ in the input line using pointer #2 (intra-highway pointer) by a round robin method</u>.

According to the present invention, it is possible to determine the VOQ in the input line at high speed because a complex algorism using the length of queue and weight, and so on is not necessary.

In Oba, the scheduling result is stored in a FiFo of the scheduling unit and read out in the First In First Out method. Oba also discloses a method for reading out the scheduling results at random as shown in Figs.8A-8D. That is, Oba does not simply use the First In First Out method to read out the scheduling results.

The structure taught by Oba for reading out the scheduling result at random has a scheduler unit including a FiFo memory storing a plurality of scheduling results, a pointer indicating a FiFo for writing and a pointer indicating a FiFo for reading out.

The scheduling result is read out at random by causing the pointers to circulate to distribute the scheduling results to the FiFo for writing the scheduling result and the FiFo for reading out the scheduling result.

In the present claimed invention the pointers defined in each of claims of the present invention are a pointer (inter highway pointer) for indicating start-of-scheduling input line and a

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pointer (intra highway pointer) for indicating VOQ that grants a read-out right by highest priority in the selected input line.

Oba does not teach the structure nor method of usage of the pointers as claimed in the present claims. The pointer defined in the claims are entirely different between the present invention and Oba.

With regard to claims 10-15, Oba discloses using a preset bandwidth weight parameter based when scheduling to fairly execute the scheduling for different bandwidth queues.

The present invention in contrast provides a load observation structure to fairly execute the scheduling for different bandwidth queues and executes the scheduling based on a result of a real load observation in a predetermined cycle.

The scheduling processing unit in applicant's claimed invention includes counts the number of packets arrived within a fixed cycle per logical forwarding request information of each input line, and performs the scheduling of a next cycle in accordance with the number of packets counted by said load observing unit.

At least these features are not found in the prior art, nor in a combination of Oba and Chao, therefore it is respectfully requested that the rejections be withdrawn.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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